

PATENT

-1-

THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Chaitanya Palusa et al.

Application No.: 09/873,016

Filed: May 30, 2001

For: DELAY SETTINGS FOR A WIDE-RANGE,
HIGH-PRECISION DELAY-LOCKED LOOP
AND A DELAY LOCKED LOOP
IMPLEMENTATION USING THESE
SETTINGS

Group No.: 2631

Examiner: Unknown

**SUBMISSION OF POWER OF
ATTORNEY BY ASSIGNEE**

121 Spear Street, Suite 290
San Francisco, CA 94105

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Technology Center 2600

Commissioner for Patents
Washington, DC 20231

Sir:

Enclosed for filing please find a duly executed Power of Attorney by Assignee for the above-identified application which specifies an Assignment recordal date of May 30, 2001, at Reel 11876, Frame 528, and shows Assignee's entire right, title and interest to establish ownership.

Respectfully submitted,

STALLMAN & POLLOCK LLP

Date: _____

9-13-2001

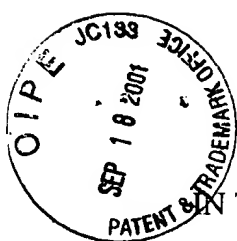
By: _____

Michael J. Pollock
Michael J. Pollock (Reg. No. 29,098)

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Atty Docket No.: ALNC-9400



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Washington, D.C. 20231

Sir:

ALLIANCE SEMICONDUCTOR CORPORATION, assignee of the entire right title and interest in the above-identified application by assignment dated December 7, 2001 and April 2, 2001, which assignment was recorded in the Patent and Trademark Office on May 30, 2001, at Reel 11876, frame 528, hereby appoints the members of the firm of STALLMAN & POLLOCK LLP, a firm composed of:

Michael A. Stallman	29,444	Kathleen A. Frost	37,326
Michael J. Pollock	29,098	Brian J. Keating	39,520

as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

Please direct all correspondence regarding this application to the following:

STALLMAN & POLLOCK LLP
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Dated: September 6, 2001

ALLIANCE SEMICONDUCTOR CORPORATION

By: 

Name: Bradley A. Perkins

Title: Vice President & General Counsel